HYS 64V16302GU
SDRAM-Modules

3.3 V 16M × 64-Bit, 128MByte SDRAM Module
168-pin Unbuffered DIMM Modules

- 168 Pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications using 256Mbit technology
- PC100-222, PC133-333 and PC133-222 versions
- One bank 16M × 64 organization
- Optimized for byte-write non-parity
- JEDEC standard Synchronous DRAMs (SDRAM)
- Single 3.3 V (± 0.3 V) power supply
- SDRAM Performance:

		-7/ -7.5	-8	Unit
		PC133	PC100	
f_{CK}	Clock Frequency (max.)	133	100	MHz
t_{AC}	Clock Access Time	5.4	6	ns

- Programmed Latencies:

Product Speed		CL	t_{RCD}	t_{RP}
-7	PC133	2	2	2
-7.5	PC133	3	3	3
-8	PC100	2	2	2

- Programmable $\overline{CAS}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs and outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes 16M × 16 (256Mbit SDRAMs in TSOPII-54 packages with 8096 refresh cycles every 64 ms
- 133.35 mm × 29.21 mm × 3.00 mm card size with gold contact pads (JEDEC MO-161)

Description

The HYS 64V16302 is an industry standard 168-pin 8-byte Dual in-line Memory Module (DIMM) which is organized as 16M × 64 in an one bank high speed memory arrays designed with 256 Mbit Synchronous DRAMs for non-parity applications. The DIMMs use -7 speed sorted 16M × 16 organised 256Mbit SDRAM devices in TSOP54 packages to meet the PC133-222 requirements, -7.5 for PC133-333 and -8 parts for the standard PC100 applications. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL’s module specification.

The DIMMs have a serial presence detect, implemented with a serial E2PROM using the 2-pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint.

Important Notice:
This module, which is based on 256MBit device technology can only be used in applications, where the 256Mbit addressing is supported.

Ordering Information

Type	Code	Package	Description	Module Height
HYS 64V16302GU-7-D	PC133-222-520	L-DIM-168-32	133 MHz CL=2 16M × 64 one bank SDRAM module	
HYS 64V16302GU-7.5-C2 HYS 64V16302GU-7.5-D	PC133-333-520	L-DIM-168-32	133 MHz CL=3 16M × 64 one bank SDRAM module	1.15”
HYS 64V16302GU-8-C2	PC100-222-620	L-DIM-168-32	100 MHz CL=2 16M × 64 one bank SDRAM module	1.15”

Note: *All part numbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS64V16302GU-8-C2, indicating Rev.C2 dies are used for SDRAM components.*

Pin Definitions and Functions

A0 - A12	Address Inputs	CLK0 - CLK3	Clock Input
BA0, BA1	Bank Select	DQMB0 - DQMB7	Data Mask
DQ0 - DQ63	Data Input/Output	$\overline{\text{CS0}}$, $\overline{\text{CS2}}$	Chip Select
CB0 - CB7	Check Bits (x72 organization only)	V_{DD}	Power (+ 3.3 V)
$\overline{\text{RAS}}$	Row Address Strobe	V_{SS}	Ground
$\overline{\text{CAS}}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{\text{WE}}$	Read/Write Input	SDA	Serial Data Out for Pres. Detect
CKE0	Clock Enable	N.C./DU	No Connection

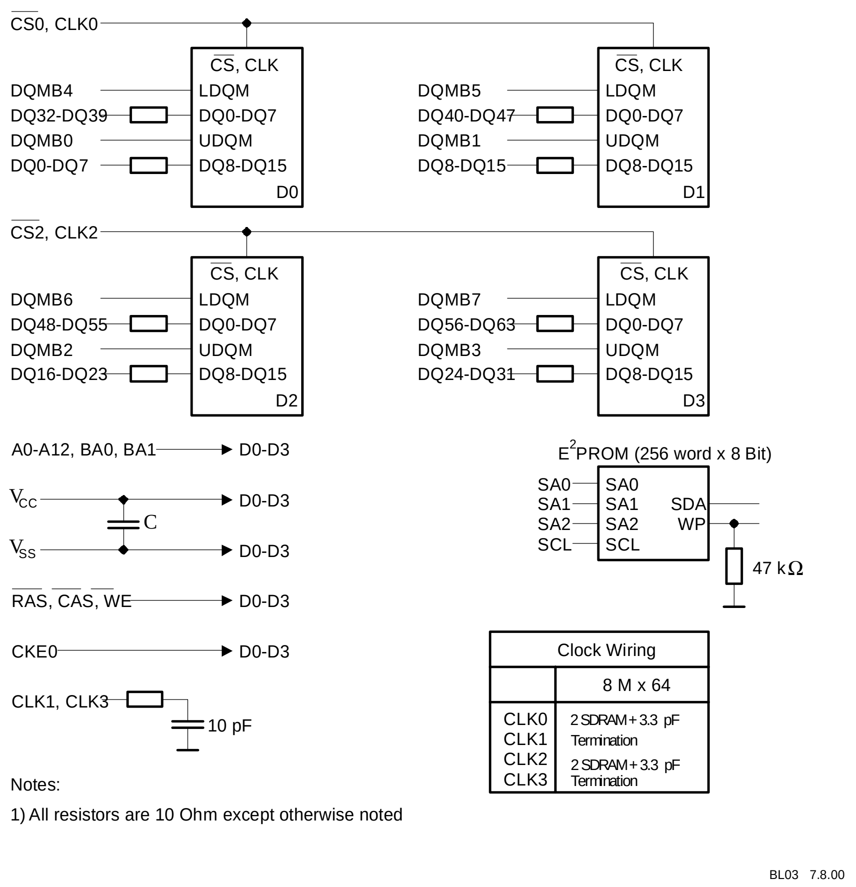
Address Format

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
16M×64	HYS64V16302GU	13	9	2	8k	64 ms	7,8 µs

Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	N.C.
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DU	90	V_{DD}	132	N.C.
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	N.C.	94	DQ39	136	CB6
11	DQ8	53	N.C.	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	N.C.	63	N.C.	105	N.C.	147	N.C.
22	N.C.	64	V_{SS}	106	N.C.	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{\text{WE}}$	69	DQ24	111	$\overline{\text{CAS}}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	N.C.	156	DQ59
31	DU	73	V_{DD}	115	$\overline{\text{RAS}}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{DD}	126	A12	168	V_{DD}

Functional Block Diagrams



Clock Wiring	
	8 M x 64
CLK0 CLK1	2 SDRAM + 3.3 pF Termination
CLK2 CLK3	2 SDRAM + 3.3 pF Termination

Notes:

1) All resistors are 10 Ohm except otherwise noted

Block Diagram: 16M x 64 One Bank SDRAM DIMM Modules (HYS 64V16302GU)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	$V_{IN,}$ V_{OUT}	– 1.0	4.6	V
Power supply voltage on V_{DD}	$V_{DD,}$	– 1.0	4.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation	P_D	–	4	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}= 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5	0.8	V
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 10	10	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values	Unit
		max.	
Input Capacitance (A0 - A12, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C_{I1}	35	pF
Input Capacitance ($\overline{\text{CS0}}$,$\overline{\text{CS2}}$)	C_{I2}	25	pF
Input Capacitance (CLK0 - CLK3)	C_{ICL}	35	pF
Input Capacitance (CKE0)	C_{I3}	30	pF
Input Capacitance (DQMB0 - DQMB7)	C_{I4}	13	pF
Input /Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	pF
Input Capacitance (SCL, SA0-2)	C_{SC}	8	pF
Input /Output Capacitance	C_{SD}	10	pF

Operating Currents per SDRAM component
T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V

Parameter	Test Condition	Symbol	-7.5	-8	Unit	Note
			max.			
Operating current $t_{RC} = t_{RC(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL=3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1}	230	170	mA	[1]
Precharge standby current in Power Down Mode $\overline{\text{CS}} = V_{IH\ (MIN.)}$, CKE $\leq V_{IL(MAX.)}$	t_{CK} = min	I_{CC2P}	2	2	mA	[1]
Precharge stand-by current in Non Power Down Mode $\overline{\text{CS}} = V_{IH\ (MIN.)}$, CKE $\geq V_{IH(MIN.)}$	t_{CK} = min	I_{CC2N}	40	30	mA	[1]
No operating current t_{CK} = min., $\overline{\text{CS}} = V_{IH\ (MIN.)}$, active state (max. 4 banks)	CKE $\geq V_{IH(MIN.)}$	I_{CC3N}	50	45	mA	[1]
	CKE $\leq V_{IL(MAX.)}$	I_{CC3P}	10	10	mA	[1]
Burst Operating Current t_{CK} = min Read command cycling	–	I_{CC4}	170	120	mA	[1, 2]
Auto Refresh Current t_{CK} = min Auto Refresh command cycling	–	I_{CC5}	150	100	mA	[1]
Self Refresh Current Self Refresh Mode CKE = 0.2 V		I_{CC6}	3	3	mA	[1]

1. All values are shown per one SDRAM component.
2. These parameters depend on the cycle rate. These values are measured at 133 MHz operation frequency for-7 & -7.5 and at 100 MHz for -8 modules.
   Input signals are changed once during t_{CK}, excepts for I_{CC6} and for stand-by currents when t_{CK} = infinity.
3. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 are assumed and th data-out current is excluded.

AC Characteristics 1), 2)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values						Unit	Note
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max	min.	max.	min.	max.		
Clock									
Clock Cycle Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	t_{CK}	 7.5 7.5	 – –	 7.5 10	 – –	 10 10	 – –	 ns ns	–
System Frequency $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	f_{CK}	 – –	 133 133	 – –	 133 100	 – –	 100 100	 MHz MHz	–
Clock Access Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	t_{AC}	 – –	 5.4 5.4	 – –	 5.4 6	 – –	 6 6	 ns ns	3), 4)
Clock High Pulse Width	t_{CH}	2.5	–	2.5	–	3	–	ns	4)
Clock Low Pulse Width	t_{CL}	2.5	–	2.5	–	3	–	ns	4)
Setup and Hold Times									
Input Setup Time	t_{CS}	1.5	–	1.5	–	2	–	ns	5)
Input Hold Time	t_{CH}	0.8	–	0.8	–	1	–	ns	5)
Power Down Mode Entry Time	t_{SB}	–	1	–	1	–	1	CLK	6)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	1	–	CLK	7)
Mode Register Setup Time	t_{RSC}	2	–	2	–	2	–	CLK	
Transition Time (rise and fall)	t_T	1	–	1	–	1	–	ns	–
Common Parameters									
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	t_{RCD}	15	–	20	–	20	–	ns	–
Precharge Time	t_{RP}	15	–	20	–	20	–	ns	–
Active Command Period	t_{RAS}	42	–	45	100k	50	100k	ns	–
Cycle Time	t_{RC}	60	–	67.5	–	70	–	ns	–
Bank to Bank Delay Time	t_{RRD}	14	–	15	–	16	–	ns	–
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time (same bank)	t_{CCD}	1	–	1	–	1	–	CLK	–

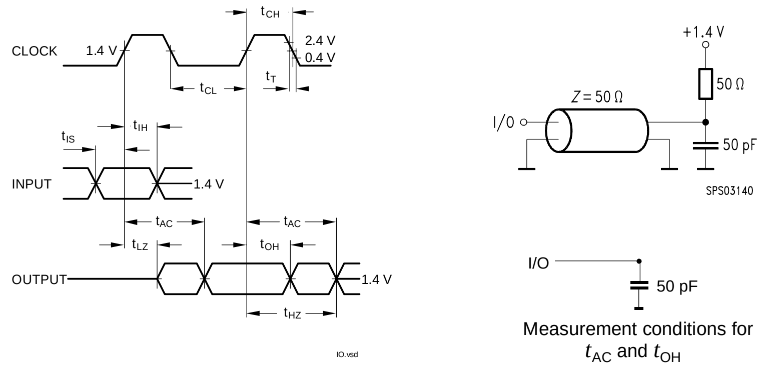
AC Characteristics (cont'd) 1), 2)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values						Unit	Note
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max	min.	max.	min.	max.		
Refresh Cycle									
Refresh Period (8192 cycles)	t_{REF}	64	–	–	64	–	64	ms	6)
Self Refresh Exit Time	t_{SREX}	–	1	1	–	1	–	CLK	8)
Read Cycle									
Data Out Hold Time	t_{OH}	3	–	3	–	3	–	ns	2)
Data Out to Low Impedance	t_{LZ}	0	–	0	–	0	–	ns	–
Data Out to High Impedance	t_{HZ}	3	7	3	7	3	8	ns	9)
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	CLK	–
Write Cycle									
Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	CLK	–

Notes

1. All AC characteristics are shown for the SDRAM components.
   An initial pause of 100 µs is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in Figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V/ns edge rate between 0.8 V and 2.0 V.
3. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns must be added to this parameter.
4. Rated at 1.4 V.
5. If t_T is longer than 1 ns, a time (t_T – 1) ns must be added to this parameter.
6. Whenever the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
7. Timing is a asynchronous. If setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.
8. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
9. This is referenced to the time at which the output achieved the open circuit condition, not to output voltage levels.



Measurement conditions for t_{AC} and t_{OH}

Serial Presence Detect

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus).

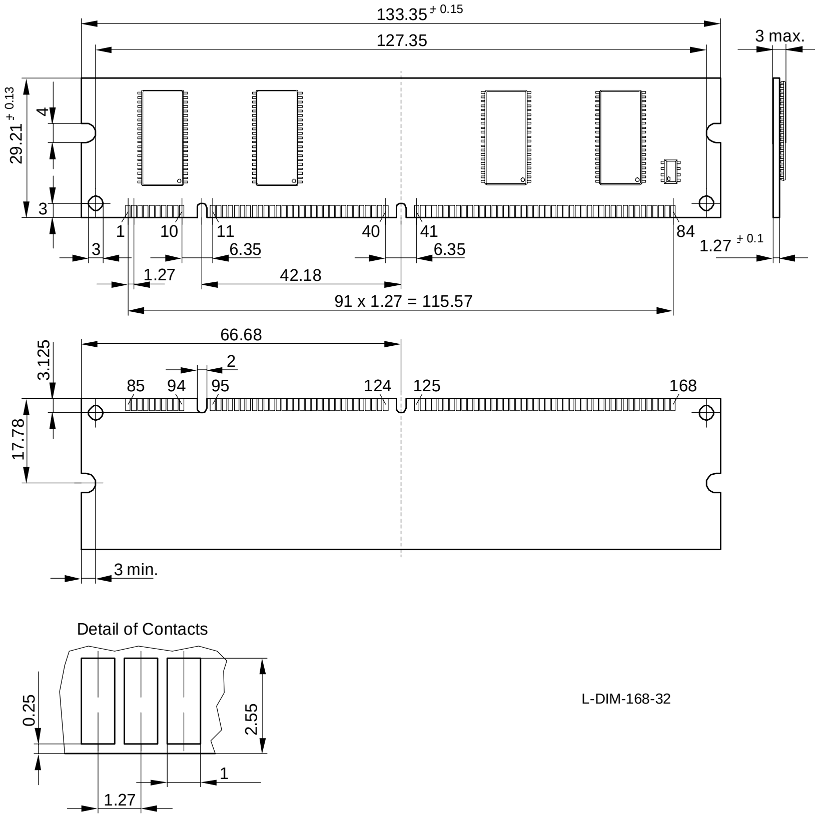
SPD-Table for 16M x 64 (128 MByte non-ECC) Modules HYS64V16302GU

Byte#	Description	SPD Entry Value	Hex		
			16M x 64		
			-7	-7.5	-8
0	Number of SPD Bytes	128	80		
1	Total Bytes in Serial PD	256	08		
2	Memory Type	SDRAM	04		
3	Number of Row Addresses	13	0D		
4	Number of Column Addresses	10	09		
5	Number of DIMM Banks	1	01		
6	Module Data Width	64	40		
7	Module Data Width (cont'd)	0	00		
8	Module Interface Levels	LVTTL	01		
9	SDRAM Cycle Time at CL = 3	7.5 / 10 ns	75	75	A0
10	SDRAM Access Time at CL = 3	5.4 / 6 ns	54	54	60
11	DIMM Config	non-ECC	00		
12	Refresh Rate/Type	Self-Refresh, 7.8 µs	82		
13	SDRAM Width, Primary	x16	10		
14	Error Checking SDRAM Data Width	na	00		
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01		
16	Burst Length Supported	1, 2, 4 & 8	0F		
17	Number of SDRAM Banks	4	04		
18	Supported $\overline{\text{CAS}}$ Latencies	CL = 2 & 3	06		
19	$\overline{\text{CS}}$ Latencies	CS latency = 0	01		
20	$\overline{\text{WE}}$ Latencies	Write latency = 0	01		
21	SDRAM DIMM Module Attributes	unbuffered	00		
22	SDRAM Device Attributes: General	V_{DD} tol +/– 10%	0E		
23	SDRAM Cycle Time at CL = 2	7.5 / 10.0 ns	75	A0	A0
24	SDRAM Access Time at CL = 2	5.4 / 6.0 ns	54	60	60
25	SDRAM Cycle Time at CL = 1	not supported	00	FF	FF
26	SDRAM Access Time at CL = 1	not supported	00	FF	FF
27	Minimum Row Precharge Time	15 / 20 ns	0F	14	14
28	Min. Row to Row Active Delay t_{RRD}	14 / 15 / 16 ns	0E	0F	10
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay t_{RCD}	15 / 20 ns	0F	14	14
30	Minimum $\overline{\text{RAS}}$ Pulse Width t_{RAS}	42 / 45 / 50 ns	2A	2D	2D
31	Module Bank Density (per bank)	256 MByte	20		
32	SDRAM Input Setup Time	1.5 / 2.0 ns	15	15	20
33	SDRAM Input Hold Time	0.8 / 1.0 ns	08	08	10
34	SDRAM Data Input Hold Time	1.5 / 2.0 ns	15	15	20
35	SDRAM Data Input Setup Time	0.8 / 1.0 ns	08	08	10

Byte#	Description	SPD Entry Value	Hex		
			16M x 64		
			-7	-7.5	-8
36-61	Superset Information	–	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12
63	Checksum for Bytes 0 - 62	–	DA	1D	7B
64	Manufacturers JEDEC ID Code	–	C1		
65-71	Manufacturer		INFINEO(N)		
72	Module Assembly Locaction				
73-90	Module Part Number				
91-92	Module Revision Code				
93-94	Module Manufacturing Code				
95-98	Module Serial Number				
99-125	Superset Information				
126	Frequency Specification		64	64	64
127	100 MHz Support Details	–	AF	AF	AF
128+	Unused Storage Locations	–	FF	FF	FF

Package Outlines

L-DIM-168-32 (JEDEC MO-161-BA)
SDRAM DIMM Module Package



Note: All tolerances according to JEDEC standard

Dimensions in mm

Change List i

1.00	Initial Release, Preliminary Information
7.00	Block Diagram changes to actual L-DIM-168-32 circuitry
7-8-2000	Clock waveform measurements on various PC133 platforms showed optimisation potential for the value of the added capacitor for each Clock Input. The 15 pF capacitor(INTEL PC100/PC133 modules specification) is not hte optimal solutio and has been changed to 3.3 pF
25-07-2001	256M S14 based modules and -7 added
06-09-2001	SCR : Absolute Maximum Rating Table added